High Temperature Silicon-on-Insulator Gate Driver for SiC-FET Power Modules

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Abstract

SiC power semiconductors have the capability of greatly outperforming Si-based power devices. Faster switching and smaller on-state losses coupled with higher voltage blocking and temperature capabilities, make SiC a very attractive semiconductor for high performance, high power density power modules. However, the temperature capabilities and increased power density are fully utilized only when the gate driver is placed next to the SiC devices. This requires the gate driver to successfully operate under these extreme conditions with reduced or no heat sinking requirements, allowing the full realization of a high efficiency, high power density SiC power module. In addition, since SiC devices are usually connected in a half or full bridge configuration, the gate driver should provide electrical isolation between the high and low voltage sections of the driver itself. This paper presents a 225 degrees Celsius operable, Silicon-On-Insulator (SOI) high voltage isolated gate driver IC for SiC devices. The IC was designed and fabricated in a 1 μm, partially depleted, CMOS process. The presented gate driver consists of a primary and a secondary side which are electrically isolated by the use of a transformer. The gate driver IC has been tested at a switching frequency of 200 kHz at 225 degrees Celsius while exhibiting a dv/dt noise immunity of at least 45 kV/μs.

Key words: gate driver, high temperature electronics, power modules

I. Introduction

SiC power devices offer a tremendous advantage over conventional switch technology, including the possibility for 10× the power density, 10× the breakdown voltage, 1/10th the switching losses, higher switching frequencies, and operation at considerably higher temperatures [1], [2]. All these properties also allow the integration of different electrical systems that previously could not operate at high temperatures.

SiC based JFETs and MOSFETs are the most common devices used for the power electronic modules in discussion, mainly since they are the most mature SiC switching structures available. By operating these devices at high ambient temperatures (250 °C+), the magnitude and complexity of the heat removal system is decreased, resulting in an increase in the power density.

The full potential of SiC power devices cannot be achieved without the presence of control circuitry to operate them in these extreme environments. However, in order fully exploit the properties of the SiC devices; the control and gate drive circuitry needs to be placed near the devices themselves to reduce parasitic inductance, and therefore increase switching speed. As an added benefit, this technology will allow for even further area miniaturization and increased power density in the final module. A critical feature of the control circuitry is also the ability to drive SiC devices connected in half bridge or full bridge configurations in order to drastically increase the number of power electronics applications of the final module.

The High Temperature Silicon-on-Insulator (HTSOI) gate driver IC reported here addresses all the previously mentioned requirements. The gate driver IC is able to: 1) operate at an ambient temperature of 225 °C, 2) provide high voltage input to output isolation and high voltage transient immunity, 3) provide device failure protection, and 4) includes advanced features such as a Pulse Width Modulator (PWM) generator on-chip.

II. HTSOI Gate Driver IC

Different gate drivers have been proposed in the last few years for the applications discussed in [3-5]. From these gate drivers, only [3] and [5] report temperatures of operation at 200 °C. However, [3] is based on a commercially available opto-isolated gate driver in addition to off-chip components which does not fully qualify for a high temperature IC design. The gate driver in [5] on the other hand, does not provide indication of any isolation method, restricting the use of the gate driver to only one switching device referenced to ground (i.e., the low-side switch).

The proposed HTSOI Gate Driver IC is an isolated gate driver capable of driving the upper and lower power transistors of a half-bridge configuration power circuit. The gate driver IC consists mainly of a primary and a secondary side; electrically isolated using a transformer and is able to operate in temperatures of up to 225 °C. In addition, protection circuits and a PWM generator are part of the IC Gate driver as well. Figure 1 shows a conceptual representation of the HTSOI Gate Driver IC and a SiC FET half bridge power module.

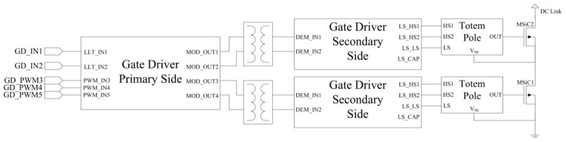


Figure 1. Conceptual representation of the HTSOI gate driver ASIC and a SiC FET power module.

The secondary side of the gate driver IC drives an external SiC totem-pole output stage for better current capability. The output stage is the one connected directly to the power devices in the half/full bridge configuration. Since there are two devices in a half-bridge configuration, a secondary side is needed to drive each device. Figure 2 shows the block diagrams of the primary and secondary sides of the HTSOI gate driver IC.

As mentioned earlier, the primary and secondary sides are electrically isolated by the use of a transformer. The external inputs to the gate driver IC are applied to the primary side and from there, the signals flow through the transformer until the outputs of the secondary side are generated. A detailed description of each circuit in both sides of the gate driver IC follows.

III. HTSOI Gate Driver IC Primary Side

A. *Logic Level Translator with hysteresis*

The Logic Level Translator (LLT) is basically a voltage step up/down circuit. It will receive a pulse input signal with a peak-to-peak value of 3.3 V or 5 V and convert it to an inverting output signal with a peak-to-peak of 5 V or 3.3 V, respectively.

The inputs to the LLT are signals coming from long distances and noisy environments. Therefore, a hysteresis circuit (Schmitt trigger) was added to the inputs of the LLT. Since this circuit is very small and sensitive to its transistor sizes, a buffer was needed between the circuit and the actual LLT.

The buffer after the hysteresis circuit consists of four inverters in series with proportional increasing sizes in their width and length ratios. The hysteresis circuit is based on a Schmitt trigger circuit where the hysteresis depends almost exclusively on the threshold level of the input inverter.

The input high level voltage (VIH) and the input low level voltage (VIL) were the values used to determine the hysteresis band. In the case of a 5 Vp-p signal, these values are approximately 3.5 V and 1.5 V. For a 3 Vp-p signal they were approximately 2.31 V and 0.66 V. The HTSOI gate driver IC makes use of two LLTs on its primary side. The outputs of the LLTs are used as control signals for the PWM conditioner.

B. *Pulse Width Modulator (PWM) conditioner*

The purpose of the PWM conditioner is to provide non-overlap protection and basic fault handling capabilities to the higher level gate driver circuitry. It is composed of a D flip-flop (D-FF) and digital logic.

When a fault is detected in the system, a signal will be sent to the D-FF which will latch into the fault state. This signal will turn off the power devices and notify the controller that a fault has occurred. When the fault clears, a signal will be sent to the D-FF which will latch out of the fault state. This signal can come from an external controller.

C. *Modulator*

The modulator, as the name states, modulates the signals to be sent across the transformer. The modulator consists of a Voltage-Controlled Ring Oscillator (VCO) and some digital logic. The VCO uses a single-ended ring of current-starved inverters and a D-FF in order to produce differential signals. The use of the D-FF allows the duty cycle of the VCO to remain fairly stable regardless of the frequency changes.

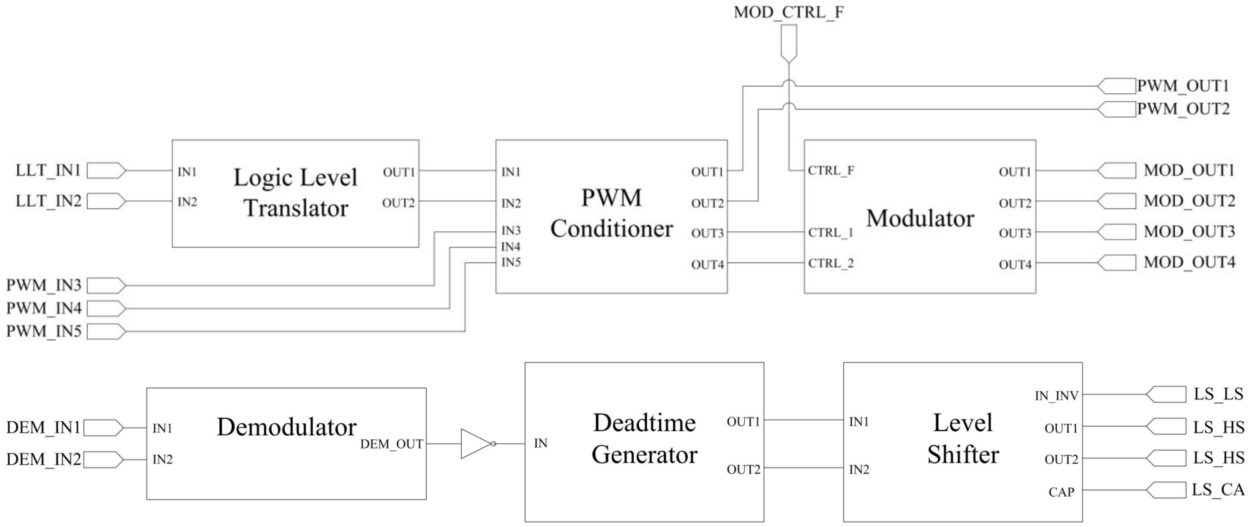


Figure 2. Primary (top) and secondary (bottom) sides of the presented HTSOI Gate Driver IC.

The current-starved inverters used in the VCO allow controlling the oscillating frequency using an external voltage input CTRL_F. Using an additional current source and sink in series with the PMOS and NMOS of the inverter respectively, the current that flows through the inverter can be limited by controlling the gate voltage of the current source and sink transistors.

The two outputs of the VCO are each connected to one input of two different NOR gates. The remaining input of the NOR gates is controlled by the PWM conditioner. The modulator outputs are buffered in order to provide the current necessary to drive the transformer.

IV. HTSOI Gate Driver IC Secondary Side

A. Demodulator

The demodulator transforms the differential oscillating signals received from the transformer into the original PWM logic signal. The demodulator consists of an envelope follower which can be tuned externally to accommodate different carrier frequencies and allow the user to trade off propagation delay for noise immunity. The envelope follower is followed by three size-scaled inverters acting as a buffer.

B. Dead time generator

The dead-time generator (DTG) will receive a pulse input signal and provide two non-overlapping output signals, one is the inverse of the other. The DTG makes use of the basic principle of using two NOR gates and one inverter to produce two non-overlapping signals. However, due to the need of considerable dead-time (to avoid shoot-through at the output stage), chains of delay circuitry in conjunction with NOR/OR gates were used throughout the circuit. These chains are composed of current-starved inverters with internal capacitors.

C. Level Shifter

The output stage of the gate driver is composed of two SiC JFETs connected in a totem-pole configuration. The use of n-channel devices in the high side of the output stage requires a higher voltage on the gate than the power rail voltage supply to turn the device on (Vgs > Vt). The bootstrap capacitor allows this to happen. The bootstrap capacitor provides two output signals connected to the gate and source of the upper NMOS device. These two signals have $\Delta V = 5$ V above the power supply to be able to turn on the device. The two output signals float depending on the driver's power supply. The inverter provides a 5 V differential signal for the low side of the output stage except that in this case, the source of the low side transistor is referenced to ground.

The two digital input signals are the same frequency and duty cycle as the PWM signal used to control the entire gate driver. The input signals are non-overlapping signals with a dead-time in between.

The bootstrap capacitor circuit is mainly composed of two diodes and an external capacitor of 100 nF connected from pad LS_CAP to pad LS_HS1 . A standard chain of inverters provides 0 to 5 V pulses to the gate of the low side transistor. Both power MOSFETs alternate their on and off state since they cannot and should never be on at the same time (due to the dead time between the two input signals to the level shifter).

V. PWM generator

The PWM generator consists of two main circuits: an oscillator and the PWM digital logic. A block diagram of these circuits is shown in Figures 3 and 4. The oscillator generates a square wave oscillating signal using an external capacitor and resistor. The PWM digital logic makes use of the oscillating signal and a ramp signal (also generated by the oscillator) together with some logic related to a leading edge blank (LEB) control signal to generate the actual PWM output signal. The maximum duty cycle and the frequency of the PWM output signal are controlled by the external resistor and capacitor, respectively.

The oscillator was implemented using two comparators monitoring the charging and discharging of a capacitor from a constant current source. The signals generated by the comparators were used to set and reset a D-FF which output is the oscillator output. The capacitor charging/discharging curves are ramp signals used by the PWM digital logic. The charging and discharging of the capacitor has some range limitations (from about 1.5 to 3.5V) due to the input common mode range of the comparator in use.

The LEB and EAOUT control signals in the PWM digital logic as shown in Figure 3 are external. EAOUT controls the pulse width of the output signal.

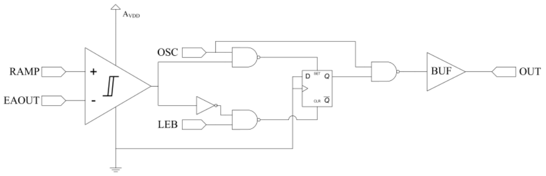


Figure 3. PWM logic circuit diagram.

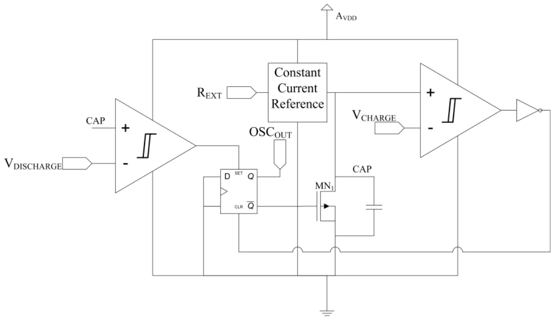


Figure 4. Oscillator circuit within the PWM generator.

The PWM generator was individually tested across temperature. The results for different capacitor and resistor values are shown in Figures 5 and 6, respectively.

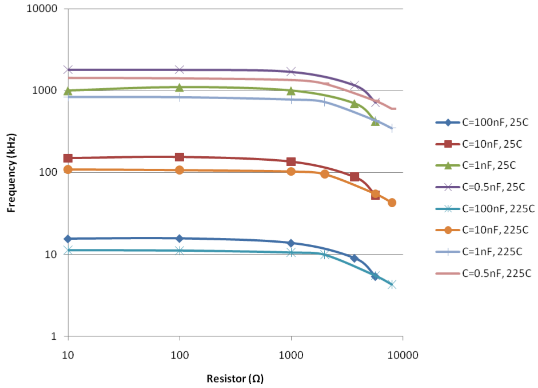


Figure 5. Frequency selection for different capacitor values across temperature.

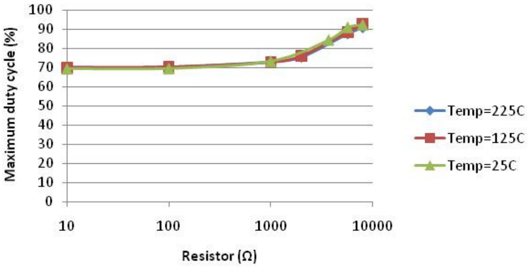


Figure 6. Maximum duty cycle selection for different resistor values across temperature.

VI. Protection Circuitry

Implemented along with the gate driver were two protection circuits, overcurrent protection and undervoltage lockout. These circuits function to ensure the proper operation of the power module as a whole by providing feedback information from key points in the system. The feedback signals are designed to be input to the power module's microcontroller, which would then take appropriate action.

A. *Overcurrent Protection*

The overcurrent protection (OCP) circuit monitors the current through the power devices and trips when the current exceeds a preset threshold. The current is monitored using a small external sensing resistor, RSENSE, placed in series with the power stage between the low side device and ground. RSENSE is sized so that the voltage drop across it is detectable when the maximum expected current flows through the power stage. The OCP propagation delay is less than 100 ns. The OCP also includes a leading-edge blanking (LEB) sub-circuit which disables an invalid OCP output when high currents are expected during switching. With the gate driver's PWM signal as its input, the LEB is able to anticipate when high currents are expected.

The OCP circuit is a comparator-based circuit, using a high-speed comparator previously designed in the same HTSOI process. Figure 7 shows a system level block diagram of the OCP circuit.

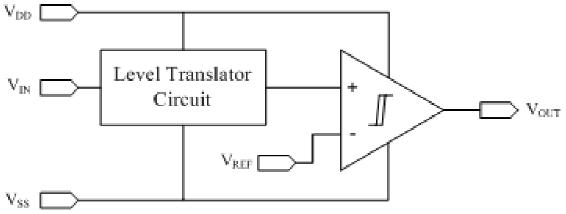


Figure 7. OCP block diagram.

The LEB circuit was designed to be programmable through an external capacitor, CLEB, relying on the capacitor's mostly linear initial charging and RC time constant. Figure 8 shows the relation between the external capacitor and the pulse width for the LEB across temperature.

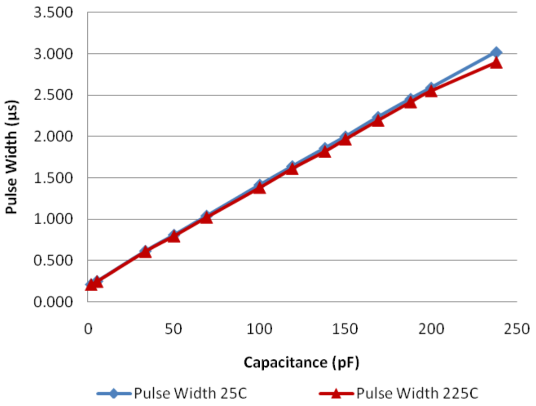
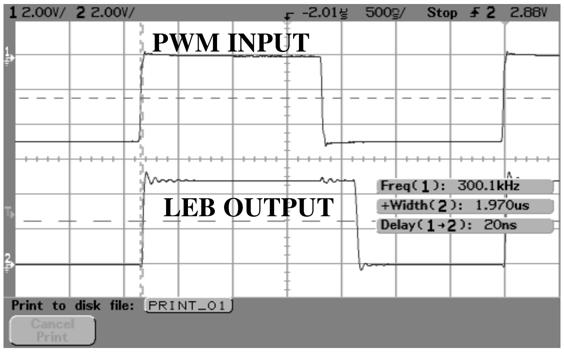


Figure 8. LEB pulse width test results across temperature.

The LEB circuit is comparator and D-FF based. The PWM signal sets the D-FF, thus beginning the blanking time and the charging of CLEB. A comparator monitors the CLEB's voltage against a reference voltage, of which the pulse width is also a function, resetting the DFF once the reference is exceeded. This ends the blanking time and discharges CLEB. Figure 9 shows the LEB operating at 225 °C generating a 1.97 µs blanking time.



Freq(1): 300.1kHz
+Width(2): 1.970us
Delay(1→2): 20ns

Figure 9. LEB at 225 °C with C_{LEB}=150 pF.

B. Undervoltage Lockout

The undervoltage lockout (UVLO) circuit monitors the chip power supply to determine whether sufficient voltage levels are present for proper circuit operation. This is especially important in startup conditions and battery powered applications where there is some decay in the power supply levels. This protection must include hysteresis to provide immunity to slowly changing or noisy input signal which can produce a noisy output if unaddressed. The UVLO circuit also includes an active pull-down (APD) sub-circuit that pulls low a node connected to VDD through a 10 kΩ pull-up resistor. Figure 10 shows the schematic of the UVLO.

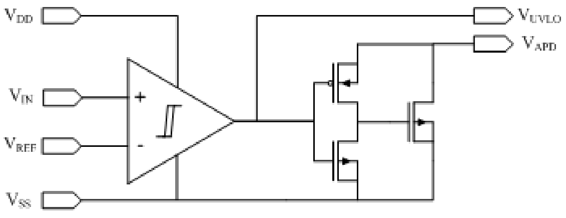


Figure 10. UVLO and APD circuit schematic.

The UVLO was designed to output low until its power supply exceeds a given voltage threshold. Once that threshold is exceeded, the circuit outputs high until the supply drops below the threshold. The UVLO was designed to have a threshold of 4.5 V with a hysteresis band of ±50 mV. When the UVLO output is low the APD circuit must be able to pull down a node to a value no greater than a pre-determined one, and when high it must allow the node to move freely. The UVLO function was realized by use of a high-speed comparator. The APD circuit was implemented as a self-biased current sink enabled by the UVLO output. Figure 11 shows the UVLO operating at 225 °C following the behavior previously described. A sine wave was used to emulate the rising behavior of the power supply.

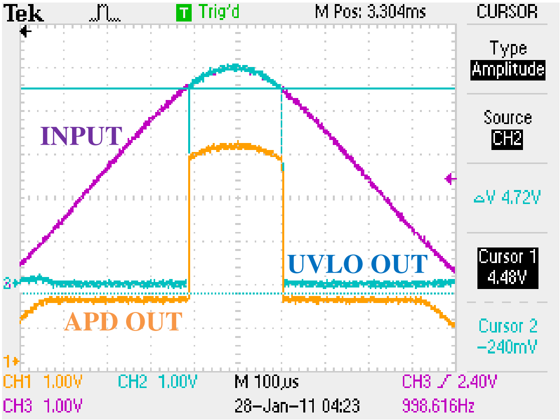


Figure 11. UVLO operating at 225 °C.

VII. Measurement Results

As mentioned before, for better current capability, the HTSOI gate driver IC secondary side was connected to a SiC totem-pole output stage with an added buffer. With the exception of this output circuitry, the Multi-Chip Module (MCM) version of the IC gate driver only requires a single IC for the primary side and a single IC for each secondary side. Figures 12 and 13 show the input and output waveforms of the gate driver ASIC operating at 200 kHz switching frequency at 25 °C and 225 °C respectively. In both cases the output has a 15 V peak-to-peak (5 V to -10 V) ideal to control normally off JFETs. The input was a 5 V peak-to-peak signal applied to the input of the LLT.

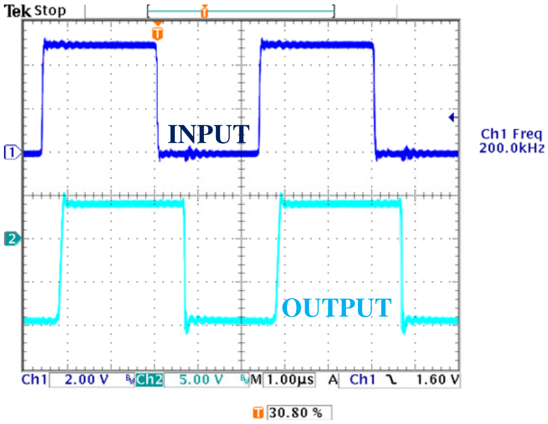


Figure 12. Gate driver ASIC at room temperature at a switching frequency of 200 kHz.

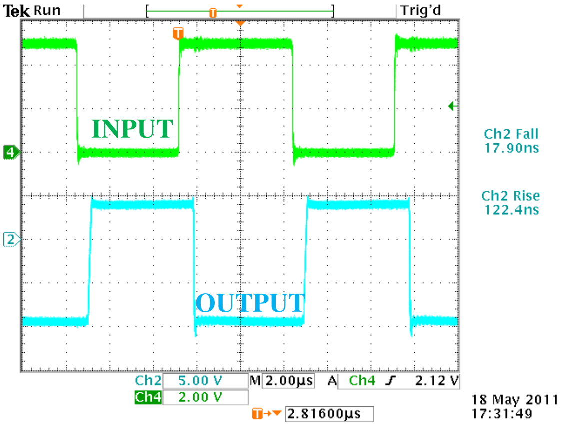


Figure 13. Gate driver ASIC at 225 °C at a switching frequency of 200 kHz.

The input to output propagation delay, jitter and rise/fall times values of the gate driver ASIC were measured to evaluate its performance and are shown in Figures 14, 15 and 16, respectively. Turn-on propagation delay varies between 625-700 ns from room temperature to 225 °C, and the turn-off delay varies from 475-625 ns. Both turn-on and turn-off jitter are less than +/- 30 ns over the temperature range. The output rise time varies from 90-140 ns and the fall time varies between 20-40 ns. In the 25 °C - 225 °C range, the fall time stays below 20 ns.

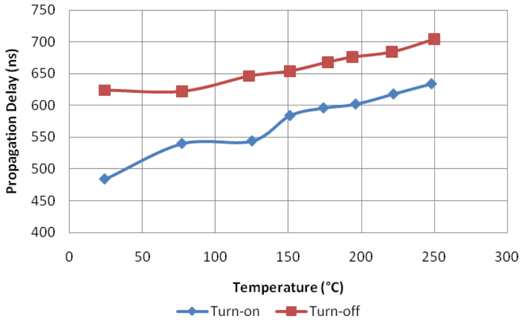


Figure 14. Propagation delay of the Gate Driver ASIC.

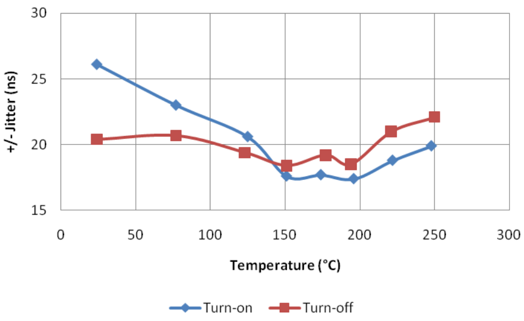


Figure 15. Jitter measurement of the gate driver ASIC.

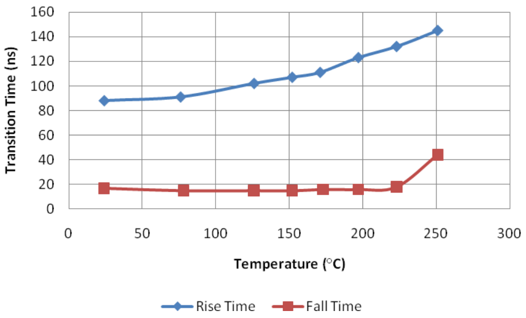


Figure 16. Output rise and fall times of the gate driver ASIC.

The isolation method used for the HTSOI gate driver IC was tested across temperature. A high speed power transistor was utilized in a clamped inductive test in order to generate the *dv/dt*. The source output of the gate driver's secondary was connected to the drain of the transistor and the ground input of the driver's primary was connected to the source of the transistor. Both turn-on and turn-off states were glitch-free at the maximum *dv/dt* capability of the test circuit, 46.8 kV/µs. Figure 17 shows the *dv/dt* measurements across temperature.

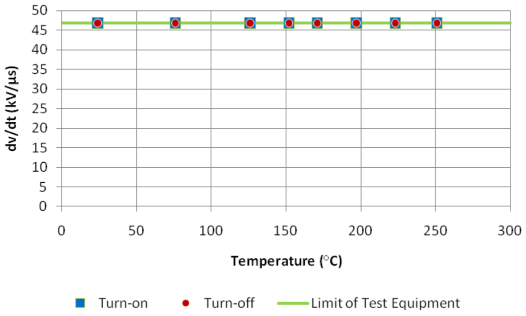


Figure 17. Gate driver ASIC *dv/dt* noise immunity.

VIII. Conclusions

In this paper, a fully integrated and isolated gate driver capable of operating at 225 °C and 200 kHz switching frequency was presented. The presented isolated gate driver IC is able to drive both the high side and low side devices in a half or full bridge power module. The prototype has been successfully tested and generated a +5/-10 V output capable of driving a normally-off SiC JFET while operating at 225 °C. In addition, the isolation feature of the gate driver was tested across temperature providing the expected noise immunity. With these features, the presented gate driver IC provides a crucial step in achieving a fully integrated and efficient power module. Future work for this gate driver IC includes the integration of the totem-pole output stage with the core circuits, as well as increasing both the switching frequency and the isolation carrier frequency. Increasing the switching frequency will allow size and weight reduction of the power stage passive components. Increasing the carrier frequency will allow faster propagation delays, improved resolution, and higher noise immunity.

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